

DEVICE AND METHOD FOR FORMING A SIGNATURE

Background Information

MISR (Multiple Input Signature Register) circuits, such as described in the publication "Built-In Test for VLSI: Pseudorandom Techniques" by Paul H. Bardell, William H. McAnney, and Jacob Savir, pp. 124 et seq., are used for forming

- 5 signatures. In circuits of this type, a given number of shift registers is provided to which data to be tested is applied in a sequence. The data occurring simultaneously is injected and shifted forward by the shift registers in a predefined cycle. After a precisely defined number of data words and cycles, there is a signature value in the shift registers which is testable and comparable with a previously known signature
- 10 value. To test a sequence, and thus the data applied, for errors, it is sufficient to compare the signature value obtained with the expected signature value. The previously known signature values may also be determined in this way.

- Problems occur with the method and the device of the related art when at a point in
- 15 time T there is an error at a certain input, because an incorrect value is then written initially into the shift register affected. The computed end signature will therefore differ from the expected signature. However, if an additional error occurs at a subsequent point in time T+1 at a subsequent, in particular directly subsequent, input, the original error at the first input is compensated again, after being shifted by
- 20 the shift registers, using a number of cycles which corresponds to the distance between the inputs and points in time, using one cycle in particular, if there is no feedback junction of the MISR, i.e., the signature generator circuit, in between. Errors occurring at such problem points in time and data word positions are thus not detected in forming the signature.

- 25 One option for taking precautions during the input to avoid this problem is to supply the inverse data word following a data word, so that an error is not compensated but detected in each case. However, this procedure doubles the number of required operations and cycles.

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